UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,233	02/11/2004	You-Cheol Shin	4591-383	4502

20575 7590 01/25/2005

MARGER JOHNSON & MCCOLLOM, P.C.
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/777,233	SHIN ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-6,8 and 9* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al., U.S. Patent No. 5,869,396 in view of Chappell et al., US Patent No. 5,541,427 B1.

Pan teaches a method of manufacturing a semiconductor device comprising the steps of:

in fig. 1, forming a gate insulating layer 14A, on a semiconductor substrate 10;

forming a silicon gate layer 16A on said gate insulating layer;

forming gate lines by patterning said silicon gate layer,

performing an impurity implantation 18a, 18b, on the semiconductor substrate using said gate lines as a mask, col. 6, line 29 - col. 7, line 36;

forming an interlayer insulating layer 22 on said substrate;

in fig. 2, exposing a surface of said silicon gate layer of said gate lines; and

in fig. 3, forming a metal silicide layer 24a, the exposed surface of said silicon gate layer, col. 8, line 16 - col. 9, line 46;

limitations from claim 2, the method of manufacturing a semiconductor device,

in fig. 4, further including the steps of forming openings to expose a given region of said substrate by partially etching said interlayer insulating layer after said step of forming said interlayer insulating layer, and filling said openings by depositing a silicon layer 28a, 28c, col. 10, lines 42-67; in fig. 2, and wherein said exposing the surface of said silicon gate layer of said gate lines includes planarizing said silicon layer, col. 8, lines 16-42;

limitations from claim 3, the method of manufacturing a semiconductor device according to claim 1, wherein said forming said metal silicide layer comprises: depositing a metal layer by a sputtering process, col. 8, lines 38-61;

annealing said metal layer; and removing non-reacted residual metal by an etching process, col. 8, line 62 - col. 9, line 46;

limitations from claim 7, in fig. 3, further comprising forming a silicide layer 24A on said planarized silicon layer, col. 8, line 62 - col. 9, line 46.

Pan does not specify using an etch stop, but Chappell does. Chappell teaches a method of manufacturing a semiconductor device, the method comprising:

in fig. 2, forming a gate insulating layer 16 on a semiconductor substrate 10;

forming a silicon gate layer 20, 24 on said gate insulating layer;

forming gate lines by patterning said silicon gate layer, col. 3, line 57 - col. 4, line 4;

performing an impurity implantation 30 by on the semiconductor substrate, using said gate lines as a mask, col. 4, lines 5-9;

in fig. 3, form an etch stop layer 34 overlying the resulting structure including the gate lines;

forming an interlayer insulating layer 40 on said etch stop layer, col. 4, lines 29-38;

in fig. 4, exposing a surface of said silicon gate layer of said gate lines through said etch stop layer, col. 5, lines 45-54; and

forming a contact layer 44B on the exposed surface of said silicon gale layer, col. 4, line 66 - col. 5, line 3. Chappell gives motivation on col. 1, lines 47-50. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chappell's invention with Pan's invention would have been beneficial because it enables a small device size with the subsequent wiring layers being relatively large in pitch.

Allowable Subject Matter

Claims 4-6, 8, 9 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: in claim 8, lines 15-18, planarizing upper portion of the gate and common source and forming metal silicide on them can not be found in the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection. Chappell teaches the newly amended features.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11 January 2005
WB

Supervisory Patent Examiner
Technology Center 2800